Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A method for programming a routing layout design, the method comprising:

(a)forming a plurality of metal traces on a first routing layer and a second routing layer; and

(b)positioning a plurality of vias within a via layer disposed between the first and second routing layers for connecting the metal traces on the first and second routing layers according to a first current route defined by a predetermined circuit layout design used for connecting a first node and a second node so as to establish a second current route equivalent to the first current route.

[c2] 2. The method of claim 1, wherein the step (a) comprises:

positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and a plurality of vertical tracks of the first routing layer respectively; and

positioning a plurality of third conducting wires and a plurality of fourth conducting wires on a plurality of hor-

izontal tracks and a plurality of vertical tracks of the second routing layer respectively, the third conducting wire on a k^{th} horizontal track of the second routing layer vertically overlapping the first conducting wire on the k^{th} horizontal track of the first routing layer.

[c3] 3. The method of claim 2, wherein the step (b) comprises:
positioning one of the vias within the via layer for electrically connecting the first conducting wire on the k^{th} horizontal track of the first routing layer and the third conducting wire on the k^{th} horizontal track of the second routing layer when the first node and the second node are electrically connected to the first conducting wire on the k^{th} horizontal track of the first routing layer and the third conducting wire on the k^{th} horizontal track of the second routing layer respectively.

[c4] 4. The method of claim 1, wherein the step (a) comprises:
positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and a plurality of vertical tracks of the first routing layer respectively; and
positioning a plurality of third conducting wires and a plurality of fourth conducting wires on a plurality of horizontal tracks and a plurality of vertical tracks of the sec-

ond routing layer respectively, the third conducting wire on an m^{th} horizontal track of the second routing layer partially overlapping the second conducting wire on an n^{th} vertical track of the first routing layer.

[c5] 5. The method of claim 4, wherein the step (b) comprises:

positioning one of the vias within the via layer for electrically connecting the second conducting wire on the n^{th} vertical track of the first routing layer and the third conducting wire on the m^{th} horizontal track of the second routing layer when the first node is electrically connected to the second conducting wire on the n^{th} vertical track of the first routing layer and the second node is electrically connected to the third conducting wire on the m^{th} horizontal track of the second routing layer.

[c6] 6. The method of claim 4, wherein the third conducting wire on the m^{th} horizontal track of the second routing layer partially overlaps the first conducting wire on the m^{th} horizontal track of the first routing layer, and the first conducting wire on the m^{th} horizontal track of the first routing layer partially overlaps the fourth conducting wire on the $n^{th}+1$ vertical track of the second routing layer.

[c7] 7. The method of claim 4, wherein the second conduct-

ing wire on the n^{th} vertical track of the first routing layer partially overlaps the fourth conducting wire on the n^{th} vertical track of the second routing layer, and the first conducting wire on the $m^{th}+1$ horizontal track of the first routing layer partially overlaps the fourth conducting wire on the n^{th} vertical track of the second routing layer.

[c8] 8. The method of claim 1, wherein the step (a) comprises:

positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the first routing layer respectively; and

positioning a plurality of third conducting wires and a plurality of fourth conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the second routing layer respectively, the fourth conducting wire on an r^{th} vertical track of the second routing layer partially overlapping the second conducting wire on the r^{th} vertical track of the first routing layer.

[c9] 9. The method of claim 8, wherein the step (b) comprises:

positioning one of the vias within the via layer for electrically connecting the second conducting wire on the r^{th} vertical track of the first routing layer and the fourth

conducting wire on the r^{th} vertical track of the second routing layer when the first node is electrically connected to the second conducting wire on the r^{th} vertical track of the first routing layer and the second node is electrically connected to the fourth conducting wire on the r^{th} vertical track of the second routing layer.

[c10] 10. The method of claim 1, wherein the step (a) comprises:

positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the first routing layer respectively; and

positioning a plurality of third conducting wires and a plurality of fourth conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the second routing layer respectively, the fourth conducting wire on an s^{th} vertical track of the second routing layer partially overlapping the first conducting wire on a t^{th} horizontal track of the first routing layer.

[c11] 11. The method of claim 10, wherein the step (b) comprises:

positioning one of the vias within the via layer for electrically connecting the first conducting wire on the t^{th} horizontal track of the first routing layer and the fourth conducting wire on the s^{th} vertical track of the second

routing layer when the first node is electrically connected to the first conducting wire on the t^{th} horizontal track of the first routing layer and the second node is electrically connected to the fourth conducting wire on the s^{th} vertical track of the second routing layer.

[c12] 12. The method of claim 10, wherein the first conducting wire on the t^{th} horizontal track of the first routing layer partially overlaps the third conducting wire on the t^{th} horizontal track of the second routing layer, and the third conducting wire on the t^{th} horizontal track of the second routing layer partially overlaps the second conducting wire on the $s^{th}+1$ vertical track of the first routing layer.

[c13] 13. The method of claim 10, wherein the second conducting wire on the s^{th} vertical track of the second routing layer partially overlaps the second conducting wire on the s^{th} vertical track of the first routing layer, and the second conducting wire on the s^{th} vertical track of the first routing layer partially overlaps the third conducting wire on the $t^{th}+1$ horizontal track of the first routing layer.

[c14] 14. The method of claim 1, wherein the metal traces on the first routing layer and the corresponding metal traces on the second routing layer have substantially the

same lengths.

[c15] 15. The method of claim 1 being applied to a multi-layer circuit board.

[c16] 16. The method of claim 1 being applied to a semiconductor device.